Circuits and Methods for Analyzing Timing Characteristics of Sequential Logic Elements

ABSTRACT

Described are systems and methods for quickly and accurately determining the set-up and hold-time requirements and clock-to-out delays associated with sequential logic elements on programmable logic devices. Programmable interconnect resources are configured to deliver signals to the data and clock terminals of each logic element under test. One or more variable delay circuits precisely place edges of the test signals on the elements of interest while a tester monitors the data clocked into the logic element to determine whether the logic element functions properly. This process is repeated for a number of selected delays.